POST-QUANTUM CRYPTOGRAPHY FOR SMALL DEVICES

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NOVEMBER 2022

SECURE CONNECTIONS
FOR A SMARTER WORLD

[1]Mostly publishing as Christine van Vredendaal

OUTLINE

- What is a smartcard?
- Why is resource constrained PQC hard?
  - Migration is hard
  - PQC is big
  - Protected PQC is bigger
  - There is not just 1 PQC
- Final thoughts

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SECURE MICROPROCESSORS – WHY DO THEY EXIST?

"For some applications, national law, corporate agreements or international standards require secure computing functions to be highly portable"

General-purpose microprocessors generally

- Do not perform modern cryptographic algorithms very well
- Are terrible at keeping their secrets to themselves during computation
- Are **unable to effectively protect stored secret data**

General chip design constraints

- Functional correctness
- Power supply
- Environmental conditions
- (not a complete list, but *nearly*)

WHAT IS A SECURE MICROPROCESSOR ANYWAY?

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- **Everything from 'general…', <u>plus</u>**

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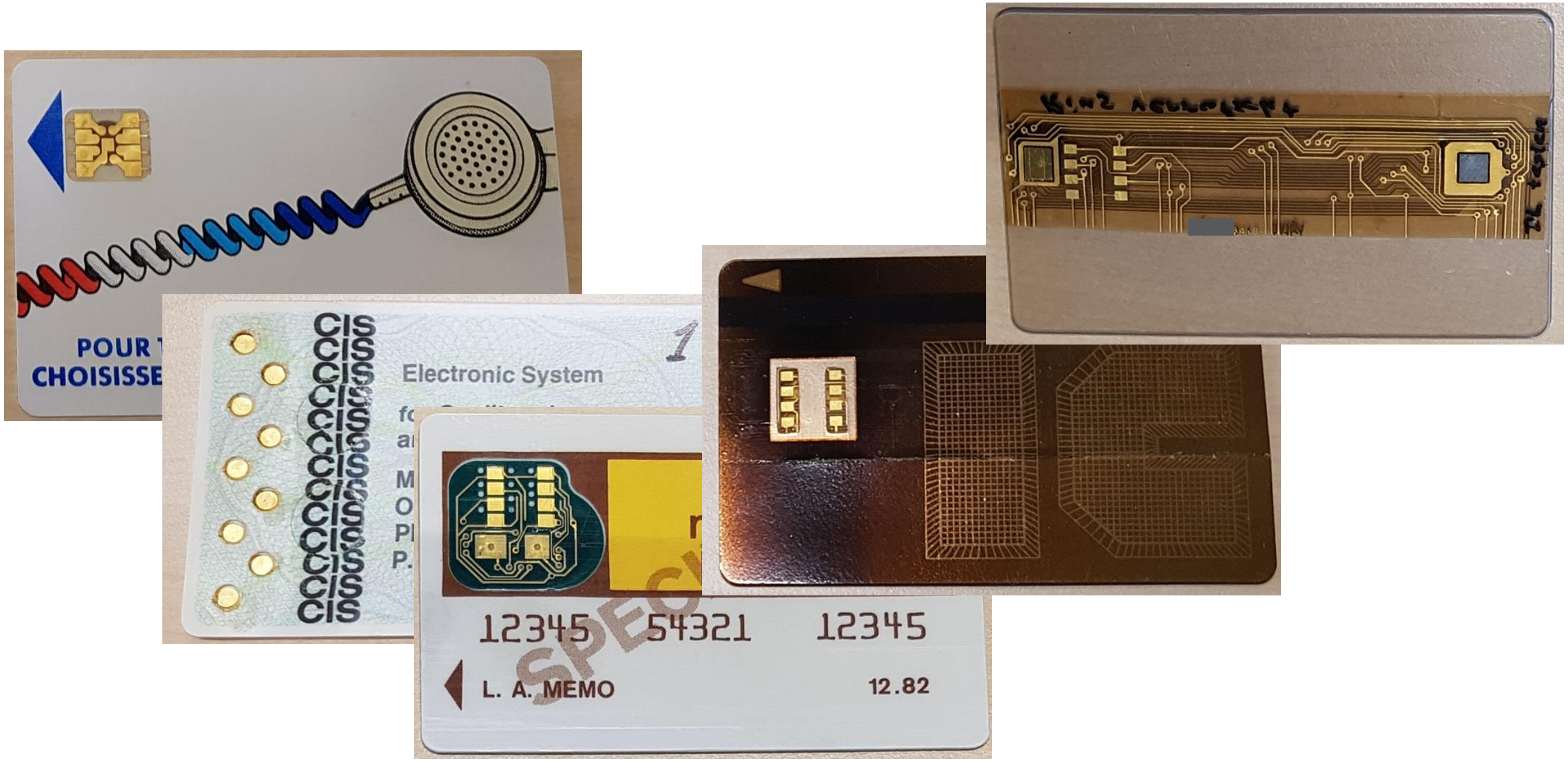
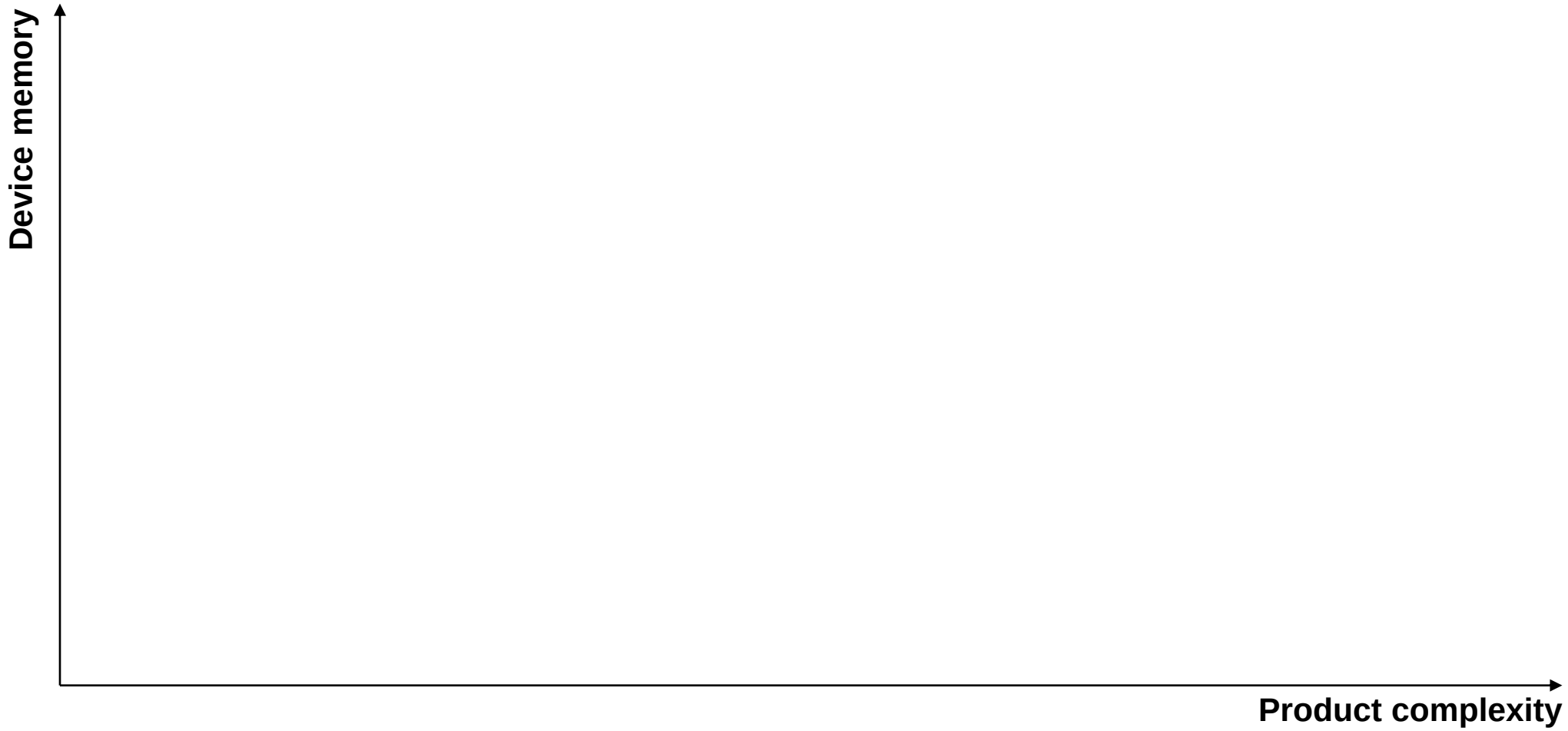
HISTORICAL EXAMPLES: EARLY 80s



NOWADAYS



NOWADAYS

Device memory

NVM: <1KB
RAM: ~64 B
Security: minimal
Not programmable

RFID

Product complexity

NOWADAYS

Device memory

NVM: 2…16KB
RAM: 4 … 8KB
Security: (Certified), Symmetric crypto
Dedicated OS and application
Contactless only

RFID

Secure µCs

(access and public transport)

Product complexity

NOWADAYS

NVM: 40…256KB
RAM: 4 … 16KB
Security: Certified, All crypto
Complex OS and applications
Contact, contactless

Device memory

Secure µCs
(identification and payment)

Secure µCs
(access and public transport)

RFID

Product complexity

NOWADAYS

Device memory

RFID

Secure µCs

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Secure µCs

(identification and payment)

eSE

NVM: 1.5…2.5MB
RAM: more
Security: Certified, All crypto
complex OS and applications
Contact (+phone), contactless
Different power supply profile

Product complexity

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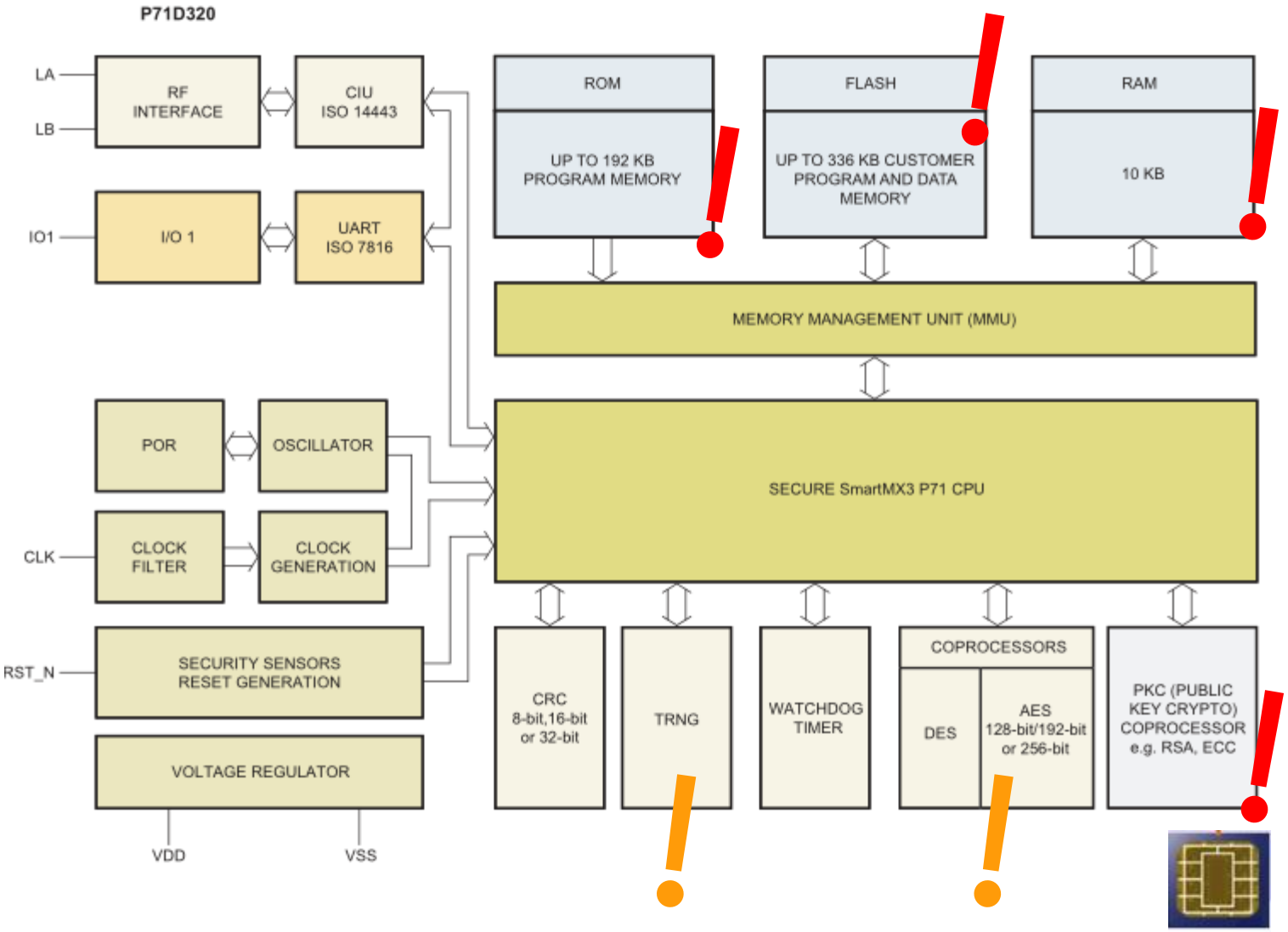
SECURE MICROPROCESSOR, EXAMPLE BLOCK DIAGRAMS



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Same product different lifetimes

One product might never migrate → does not want to pay (money, performance) for extra functionality

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Secure HW design can take a long time

Replacing the PKC block → many years of research

Adding the PKC block → extra space

Hybrid modes are not that clear

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HW has to be replaced physically

Maintaining interoperability is often vital

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(SOME) CHALLENGES OF PQC ON EMBEDDED DEVICES

Key Sizes

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- **PQC is order of magnitude larger**

PQC Signature Scheme: Crystals-Dilithium

Compared to current solution based on ECC:

Size (bytes)	**Ed25519**	**Dilithium-3**
Private key	64	**4000**
Public key	32	**1952**
Signature	64	3293

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ROM/Flash; small issues like storing many keys or **McEliece keys** with public key sizes of **255 KiB – 1,326 KiB.**

RAM; bigger issue. Many schemes use a lot of stack by default (50 – 100 KiB in pqm4).
Most secure microcontrollers are closer to 8~16 KB.

Lots of optimization necessary, impacts performance

SIGNATURE VERIFICATION – ECC VERSUS PQC

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Case Study: Signature Verification

- Secure Boot
- Secure (over-the-air) Update

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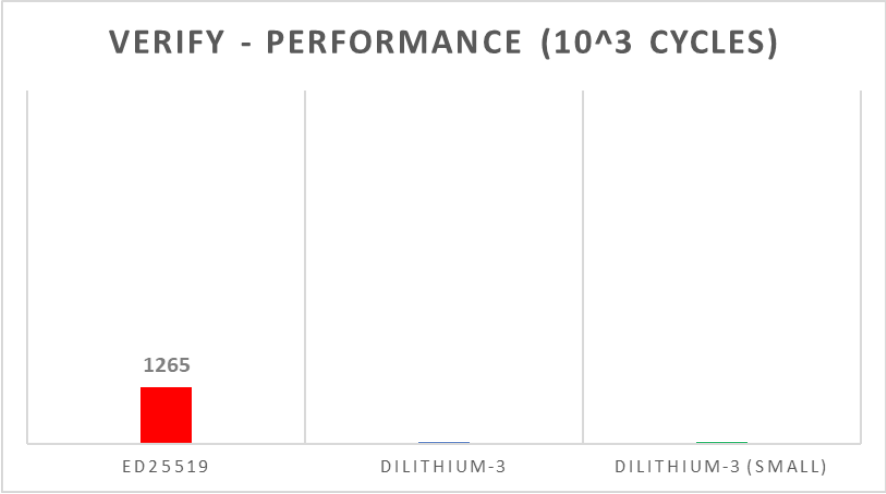
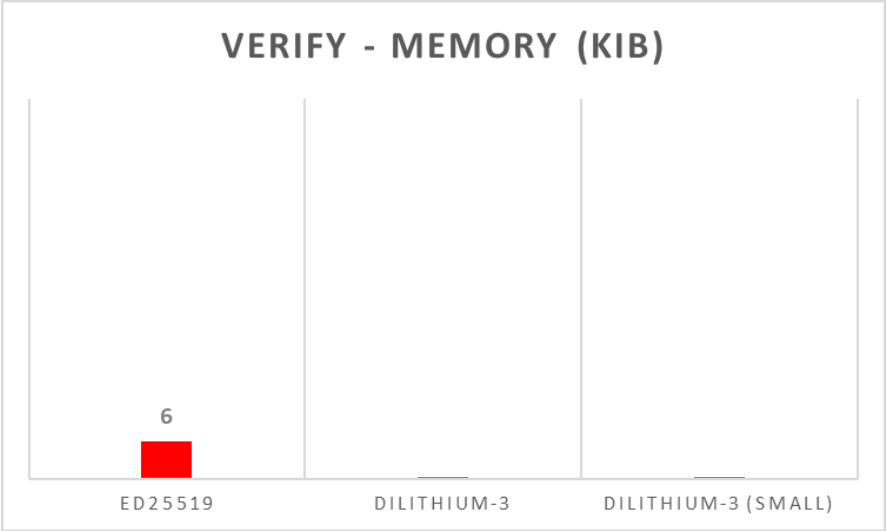
Academic figures on ARM Cortex-M4





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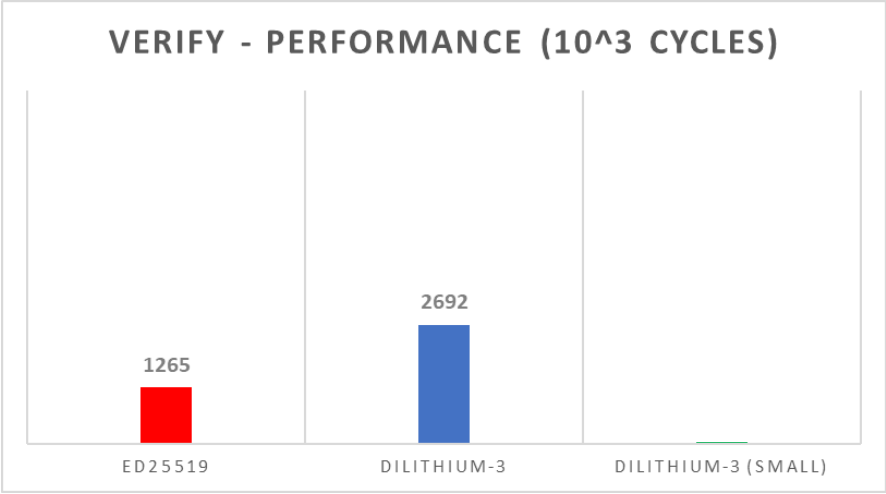

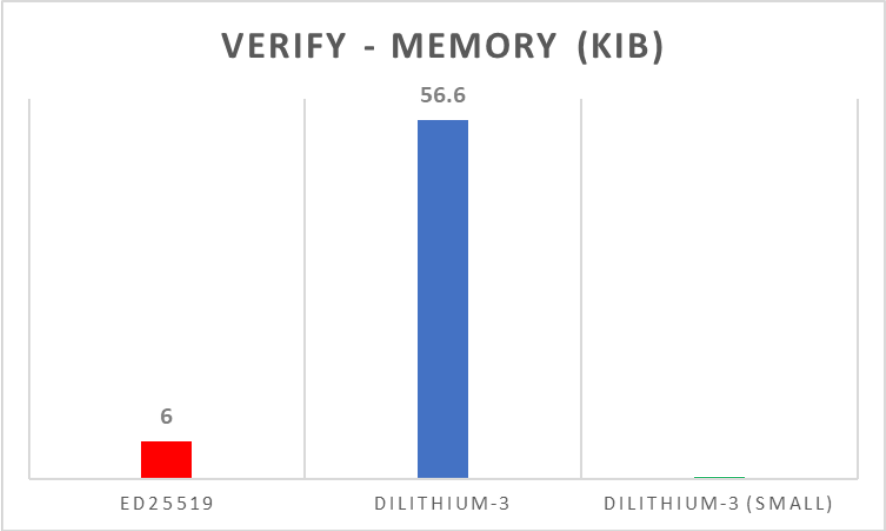

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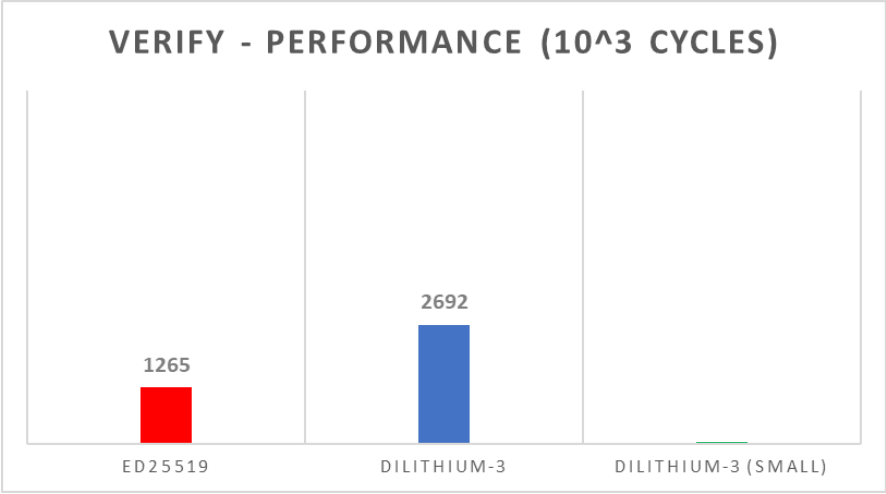

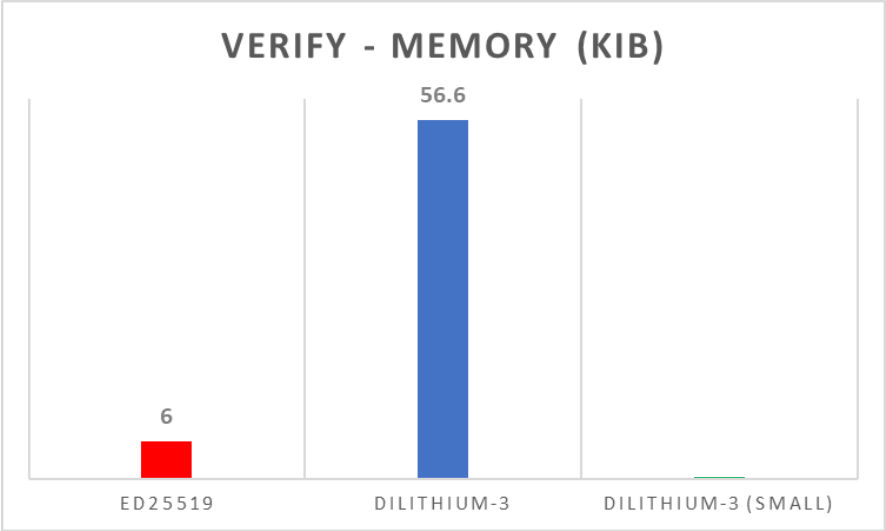

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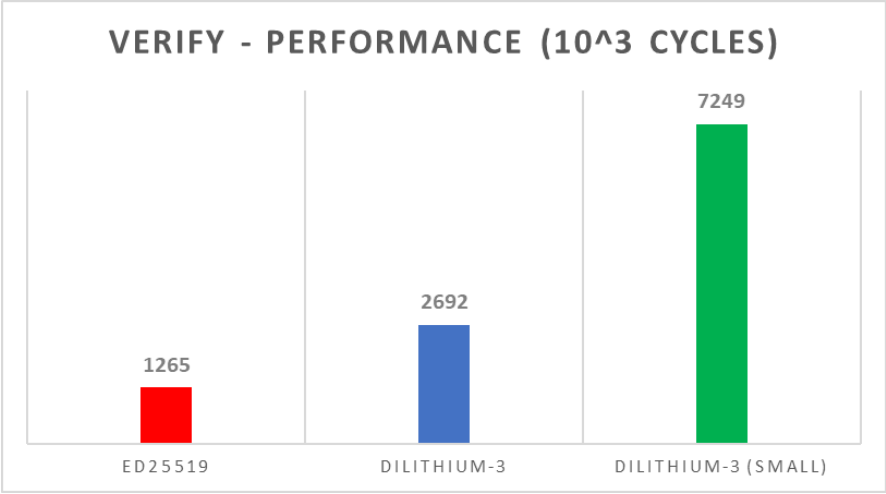
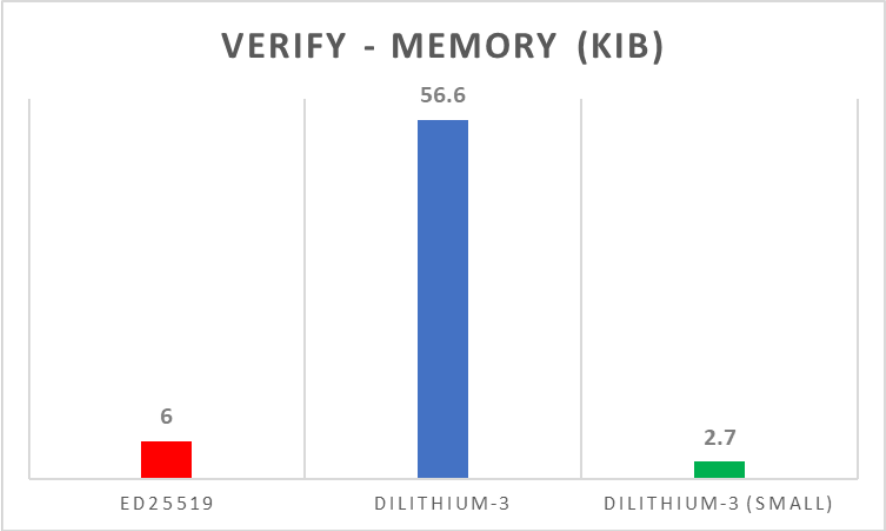
- Significant speed-up potential: SHA-3 HW acceleration





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BACK TO THE SMARTCARDS

- Smartcard CPU cores are generally less efficient than an ARM Cortex M4
  - Let's say a factor c slowdown
- Need hardening against fault attacks
  - Let's say a factor f slowdown
- Back-of-the-envelope: at least 1-second for verification
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- This does not take protocol operations into account
- Industry standard (access control, payment) ~200ms
- Hardened signing will be worse

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For ECC/RSA, SCA are quite mature and well-understood

For PQC work has started ~5 years ago

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Performance overhead compared to **unprotected** (d=1) Kyber on Cortex-M4 for high noise (SW) / low noise settings (HW + SW) [BGR+21]:

SCA security level →

d=2	d=3	d=4	d=5	d=6	d=7
3.5x	64x	110x	197x	293x	397x

[BGR+21] Bos et al.: Masking Kyber, TCHES-2021

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SCA security level

d=2	d=3	d=4	d=5	d=6	d=7	N/A*
3.5x	64x	110x	197x	293x	397x	
	High(er)					Low

18x **?**

* For this specific implementation + board.

Requires further stack usage optimization.

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So, what to support?

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Scheme	Number of schemes
Signature	1
KEM	0

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Scheme	
Signature	~~1~~ 4
KEM	~~0~~ 1

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Scheme	
Signature	~~1~~ ~~4~~ 5
KEM	~~0~~ ~~1~~ 2

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Scheme	
Signature	~~1 4~~ 5
KEM	~~0 1 2~~ 4

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- China: LAC
- Others?

Scheme	
Signature	~~1~~ ~~4~~ 5
KEM	~~0~~ ~~1~~ ~~2~~ ~~4~~ 5

???

HIGHER-LEVEL STANDARDS

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A lot of (secure microcontroller) applications follow standards

- Global Platform for trusted digital services
- Trusted Computing Group for trusted computing platforms
- IETF for Internet things
- ISO/IEC for all kinds of application domains
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What if some lag behind in setting post-quantum standards?

What if these do not agree?

What if a secure microcontroller has to support multiple?

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Irrelevant if the quantum threat is real or not.

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PQC will be a challenge.

Performance, memory, key size, hardening, migration and agility.

What will be the main challenge for your industry?

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What will be the main challenge for your industry?

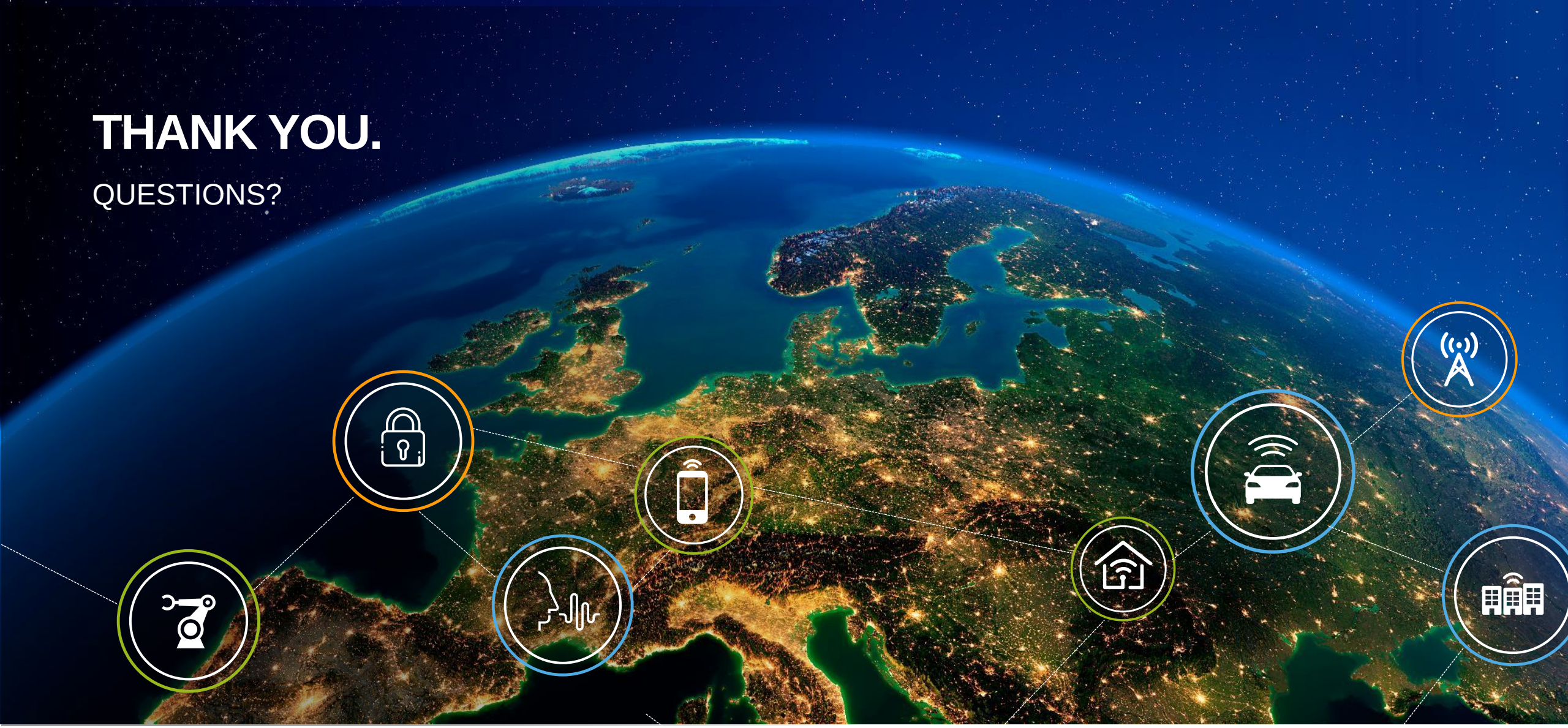
Start now.

Identify issues now, so bottlenecks can be solved.

Can serve as input for standardization.

THANK YOU.

QUESTIONS?



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CONTACT: PQC@NXP.COM | NXP.COM/PQC